REMARKS

Claims 1 and 3-18 are pending in the present application. Claim 2 is canceled herein. Claims 11-18 have been added, and claim 1 has been amended. No new matter has been added.

Claims 1-10 have been rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 6,504,777 B1 to Hsu, et al. (hereinafter "Hsu"). Applicant respectfully traverses this rejection.

Claim 1, as amended, specifically recites a RAM store in which "bit line pairs have respective charge equalization circuits individually associated with them" and "a shorting transistor is arranged in or on a respective sense amplifier (SA) jointly for all bit line pairs ... provided to connect, at the sense amplifier, the bit line halves of the bit line pairs." The charge equalization circuits are controlled by a precharge control signal and the shorting transistor is controlled by "a separate shorting control signal via a dedicated control line separately from the precharge control signal."

Applicant respectfully submits that the references of record do not teach or suggest the limitations of claim 1. For example, Hsu teaches a precharge and equalization device 50, which includes precharge and equalization transistors that are all controlled by a common signal EQL. These circuitry is not controlled by separate a shorting control signal and precharge control signal, as required by claim 1.

The Office Action points to transistor 110 (Figure 3) as a shorting transistor. Applicant respectfully submits that the transistor 110 cannot be a shorting transistor as claimed. In claim 1, the shorting transistor "is arranged in or on a respective sense amplifier." The transistor 110, on the other hand is clearly connected between lines of the master data lines MDQ and bMDQ. The master data line is clearly not part of the sense amplifier. *See e.g.*, col. 4, lines 34-36 ("The data

amplified by the first sense amplifier SA is then sent to a secondary sense amplifier SSA via a local data line LDQ to a master data line MDQ.")

Further, the "shorting transistor [is] provided to connect, at the sense amplifier, the bit line halves of the bit line pairs that are in the precharge phase." The master data line reset transistor 110, which receives data line reset signal DQRST, clearly does not connect any bit line halves at the sense amplifier. Further, the reference provides no teaching that the data line reset signal DQRST is activated when the bit line pairs are in the precharge phase.

It is therefore respectfully submitted that claim 1 is allowable over the references of record.

Claims 3-5 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claim 6, as originally filed, specifically recites "the bit line halves of the bit line pairs associated with the same sense amplifier are shorted, when these bit lines pairs are in the precharge phase on account of the precharge control signal supplied to them, by means of a shorting transistor arranged in or on each sense amplifier by supplying this shorting transistor with a dedicated shorting control signal." Applicant respectfully submits that the references of record do not teach or suggest the limitations of claim 6.

The Office Action provides absolutely no rationale as to how this claim could be anticipated by the Hsu reference. In fact, the Office Action makes no reference to the claim outside of stating that it is rejected. As a result, the Office Action clearly fails to make a *prima facie* case of unpatentability and the claim must be allowed.

Claims 7-10 depend from claim 6 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claims 11-18 have been added herein. No new matter has been added. It is respectfully submitted that these newly added claims are allowable over the references of record.

In view of the above, Applicants respectfully submit that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicants request that the Examiner contact Applicants' attorney at the address below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

2/17/06
Date

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